REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Specification, Abstract, Claims, and Drawings

The specification has been amended to correct the informality noted in paragraph 2 on page 2 of the Official Action.

In addition, the specification, abstract, and claims have been amended to place the application in proper U.S. format and to correct various minor grammatical and idiomatic errors.

Fig. 1 has been amended to label the functional blocks, as required in item 1 on page 2 of the Official Action.

Fig. 2 has been amended to indicate that the counter inputs data from the buffer in order to count the number of zeros in the temporarily stored unit data train and thereby set the state flag, as indicated in the **paragraph [0015]** of the specification, and as would be clearly understood by those skilled in the art (the purpose of the buffer is obviously to hold the data train during counting of the zeros and setting of the flag, so that the inverter unit can be set to invert or not invert the data train, which implies that the counter must be directly connected to the buffer).

Because the changes to the specification, abstract, and drawings are all formal in nature, it is respectfully submitted that the changes do not involve new matter. In addition, the changes to **claim 1** are all formal in nature and do not involve new matter, new **claim 3** is supported by the description in **line 6** on **page 4** of the original specification, and new **claim 4** is supported by the description in **lines 12-19** on **page 4** of the original specification, and therefore the amendments to the claims also do not involve new matter.

2. Rejection of Claims 1 and 2 Under 35 USC §112, 2nd Paragraph

This rejection has been addressed by:

- amending claim 1 to delete the recitation of the "operating state" in favor of a clearer recitation that the state flag indicates whether the pulse train is to be inverted (which occurs when the number of zeros exceeds a "default proportion" or threshold, as recited in the fourth paragraph of amended claim 1);
- amending claim 1 to recite "~~the~~ total bits of logic" and "~~a~~ counted result" in order to correct the antecedence errors as suggested by the Examiner;
- deleting "interpolating" (which was apparently intended to mean "interposed');
- deleting claim 2.

3. Rejection of Claims 1 and 2 Under 35 USC §102(b) in view of U.S. Patent No. 5,561,632 (Arase)

This rejection is respectfully traversed on the grounds that the Arase patent fails to disclose or suggest inclusion of inverters between a host computing device and a memory for the purpose of inverting a unit data train to be written in the memory whenever the unit data train contains a predetermined number of zeros, as recited in claim 1 (and re-inverting an inverted unit data train upon reading, as recited in claim 4). Arase does count the number of zeros, but performs no inversion in response thereto. Instead, Arase uses the number of zeros to determined when a word line should be replaced with a redundant word line.

The purpose of the invention is simply to reduce the number of zeros that are written into the memory, thereby extending the life of the memory by eliminating the need to re-write previously stored zeros with ones as part of the refresh operation used to prepare the memory for writing new data. To accomplish this, the claimed invention counts the number of zeros in a unit data train. If the number of zeros is high (50% or higher), then the unit data train is inverted so that there are fewer zeros and more ones. As a result, fewer zeros need to be written into the memory. A flag keeps track of whether the data written into the memory has been inverted, so

that inverted data can be re-inverted during reading (data that has not been inverted during writing of course does not need to be re-inverted during reading).

The Arase patent, in contrast, discloses a system which replaces word lines that have been used for a predetermined number of cycles with redundant or backup word lines. While Arase does check the number of ones and zeros, it does so in order to establish the number of cycles at which time the word line should be replaced. This is not the same as inverting the data to be written whenever the number of zeros exceeds the number of ones so as to reduce the number of zeros written into the memory. Arase does not attempt to reduce the number of zeros written into memory, but merely counts them in order to determine when a corresponding word line should be replaced.

The switching of word lines in the system of Arase does prolong the life of the memory, but it also reduces its speed. In contrast, the claimed invention actually increases the speed of the flash memory while still extending its life, because ones can be written faster than zeros (due to the "hot carriers" effect discussed in the introductory section of the present application). The claimed invention could be used in connection with the memory of Arase, by reducing the number of zeros that are stored in the memory and therefore extending the time before replacement of a word line, but such inversion is clearly not suggested by Arase. The memory of Arase stores unit data trains in the memory *irrespective* of whether the trains contain more zeros than ones, and there is no suggestion of inverting unit data trains when the "total bits of logic zero. . .outnumbers a default proportion" as claimed.

Because the Arase patent does not disclose or suggest, whether considered individually or in combination with any of the references of record, all elements recited in any of claims 1, 3, and 4, withdrawal of the rejection under 35 USC §102(b) in view of the Arase patent is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

BACON & THOMAS, PLLC

By: BENJAMIN E. URCIA
Registration No. 33,805

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BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500

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